Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A modular computer system formed by connecting a processing module having a processor mounted thereon and a plurality of I/O modules in a stacked form via connectors forming a bus, wherein

each ~~of said I/O modules~~ I/O module comprises:

a module exclusive selection part for activating the module responsive to a module select signal input from a terminal in a predetermined position on a processing module side connector, the predetermined position being the same for said I/O modules; and

an ID output part for outputting identification information of its own I/O module to a predetermined terminal on the connector on the basis of ~~a~~ the module select ~~activate~~ signal output from said module exclusive selection part;

wherein said processing module comprises:

a module select signal output part for outputting the module select signal to a connector terminal to which the I/O module is connected; and

an ID input part for taking in the identification information output to the predetermined terminal on the connector,

said module select signal output part outputs the module select signal successively to the I/O modules connected to the processing module, and

said ID input part recognizes the I/O modules and the

<u>identification information in association in accordance with an</u>

<u>output order of the module select signal; and</u>

<u>wherein in accordance with the association of the I/O modules with the</u>

<u>identification information, said processing module selects from differing preset bus</u>

<u>configuration parameters and device drivers, from a memory, for accessing differing</u>

<u>types of the I/O modules</u>.

2. - 3. (Canceled)

4. (Currently Amended) A modular computer system formed by connecting a

processing module having a processor mounted thereon and a plurality of I/O

modules in a stacked form via connectors forming a bus, wherein

each of said I/O modules <u>I/O module</u> comprises:

a module exclusive selection part for determining whether a<u>n selecting</u>

module select signal <u>of module select signals</u> input from a processing module side

<u>input</u> connector is a signal <u>on a predetermined connector terminal position of the</u>

<u>input connector,</u> that selects its own <u>the I/O</u> module, outputting an activate signal for

the module select signal, when the module select signal is the signal <u>on the</u>

<u>predetermined connector terminal position</u> that selects its own <u>the I/O</u> module, and

transmitting <u>shifting</u> the module select signals to a <u>differing</u> terminals that is included

in terminals on a<u>of an output</u> connector opposite to the processing module and that

is in the same position as that of a terminal on the processing module side

connector supplied with the signal that selects its own module. <u>in a predetermined</u>

<u>shifting</u> when the module select signal input from the processing module side <u>input</u>

connector is a signal that selects another <u>I/O</u> module; and

an ID output part for outputting identification information of its own<u>the</u>

I/O module to a predetermined terminal on the processing module side <u>input</u>

connector ~~on the basis of~~ responsive to the activate signal, wherein said ID output

part comprises: ;

> an ID generation part for generating identification

information of its own module; and

> an output enable part for outputting the identification

information generated by said ID generation part, to a

predetermined terminal on the connector; and

wherein said ID generation part generates the identification information

as a serial signal on the basis of the activate signal and a clock signal.

5. (Currently Amended) The modular computer system according to claim ~~4~~-21,
wherein

> said module exclusive selection part has a plurality of wires connected

to a plurality of connector terminals of the input connector on the processing module

side,

> one of the wires is connected to said ID output part, and

> one of other wires is connected to a terminal that is included in a

plurality of connector terminals on ~~a side opposite to the processing module~~ the

ouput connector, and that is in the same position as that of the connector terminal

supplied with a module select signal that selects its own module.

6. (Currently Amended) The modular computer system according to claim ~~4~~-21,
wherein said module exclusive selection part is formed by connecting a D terminal of
a D type flip-flop to one of connector terminals on the ~~processing module side,~~ input

connector, connecting a Q output terminal of said D type flip-flop to said ID output

part and to a terminal that is included in ~~connector terminals on a side opposite to~~

~~the processing module~~ the output connector and that is in the same position as that

of the connector terminal to which the D terminal is connected, and connecting a

clock terminal of said D type flip-flop to a terminal to which connector terminals on

the ~~processing module side and the side opposite to the processing module~~ input

connector and output connector are connected in common.

7. (Original) The modular computer system according to claim 6, wherein said

processing module drives the connector terminal to which the clock terminal is

connected, with a clock signal, and drives the connector terminal to which the D

terminal is connected, with an enable signal.

8. (Currently Amended) The modular computer system according to claim ~~4~~-21,

wherein said ID output part comprises:

        an ID generation part for generating identification information of its own

module; and

        an output enable part for outputting the identification information

generated by said ID generation part to a predetermined terminal on the input

connector.

9. (Currently Amended) The modular computer system according to claim ~~8~~-4,

wherein said ID output part comprises gate elements that are supplied with the

identification information as inputs thereof and that are enabled by the activate

signal.

10. (Currently Amended) The modular computer system according to claim ~~8~~-21,

wherein said ID generation part generates the identification information as a serial

signal on the basis of the activate signal and a clock signal.

11. (Currently Amended) The modular computer system according to claim 4.-21,
wherein said ID output part is formed by connecting wires driven by the activate
signal to a plurality of predetermined terminals on the connector via PN-junction
elements according to the identification information.

12. (Currently Amended) The modular computer system according to claim 4,
wherein said processing module comprises:

a module select signal output part for outputting the

module select signals to a-the input connector terminal-to which

the-a first I/O module is connected;

an ID input part for taking in the identification information

output to the predetermined terminal on the input connector,

said module select signal output part outputs the

selecting module select signal successively to the I/O modules

connected-coupled to the processing module, and

said ID input part recognizes the I/O modules and the

identification information in association in accordance with an

output order of the selecting module select signal.

13. (Currently Amended) The modular computer system according to claim 12,
wherein in accordance with the association of the I/O modules with the identification
information, said processing module selects from differing preset bus configuration
parameters and device drivers, from a memory, for accessing differing types of the
I/O modules. wherein-in-accordance-with-the-association-of-the-I/O-modules-with-the
identification-information,-said-processing-module-reads-preset-bus-configuration
parameters-and-device-drivers-of-the-I/O-modules-from-a-memory,-and-accesses-the
I/O-modules.

14. - 20. (Canceled)

21. (New) A modular computer system formed by connecting a processing module having a processor mounted thereon and a plurality of I/O modules in a stacked form via connectors forming a bus, wherein

each I/O module comprises:

a module exclusive selection part for determining whether a module select signal input from a processing module side input connector is a signal that selects its own module, outputting an activate signal when the module select signal is the signal that selects its own module, and transmitting the module select signal to a terminal that is included in terminals on an output connector opposite to the processing module and that is in the same position as that of a terminal on the input connector supplied with the signal that selects its own module, when the module select signal input from the input connector is a signal that selects another module; and

an ID output part for outputting identification information of the I/O module to a predetermined terminal on the input connector responsive to the activate signal;

wherein said processing module comprises:

a module select signal output part for outputting the module select signals to the input connector to which a first I/O module is connected;

an ID input part for taking in the identification information output to the predetermined terminal on the input connector,

said module select signal output part outputs the selecting module select signal successively to the I/O modules

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     coupled to the processing module, and

      said ID input part recognizes the I/O modules and the

    identification information in association in accordance with an

    output order of the selecting module select signal; and

   wherein in accordance with the association of the I/O modules with the

identification information, said processing module selects from differing preset bus

configuration parameters and device drivers, from a memory, for accessing differing

types of the I/O modules.